REMARKS/ARGUMENTS

In the Office Action mailed May 27, 2008, claims 1-8 and 10-25 were rejected. In response, Applicants hereby request reconsideration of the application in view of the below-provided remarks. No claims are amended, added, or canceled.

Claim Rejections under 35 U.S.C. 103

Claims 1-4, 7, 8, and 10 were rejected under 35 U.S.C. 103(a) as being unpatentable over Stockdale et al. (U.S. Pat. No. 6,804,763, hereinafter Stockdale) in view of Cheng et al. (U.S. Pat. No. 5,701,516, hereinafter Cheng), and further in view of O'Neill (U.S. Pat. Pub. No. 2003/0182414, hereinafter O'Neill). Additionally, claims 5, 6, and 11-15 were rejected under 35 U.S.C. 103(a) as being unpatentable over Stockdale, in view of Cheng, further in view of O'Neill and further in view of Hanes (U.S. Pat. Pub. No. 2003/0081932, hereinafter Hanes). Additionally, claims 16-25 were rejected under 35 U.S.C. 103(a) as being unpatentable over Stockdale, in view of Cheng in view of O'Neill in view of Hanes and further in view of Lee et al. (U.S. Pat. No. 5,930,167, hereinafter Lee). However, Applicants respectfully submit that these claims are patentable over Stockdale, Cheng, O'Neill, Hanes, and Lee for the reasons provided below.

Independent Claim 1

Claim 1 recites "a memory allocation unit adapted to communicate with at least one application device and to allocate at least one first part of said memory space to said application device to write a first working data structure comprising a plurality of working data blocks to the memory space and to write a second working data structure comprising a copy of the plurality of working data blocks, wherein the second working data structure comprises a copy of the first working data structure in the same memory space as the first working data structure" (emphasis added).

Applicants submit that the combination of Stockdale, Cheng, and O'Neill does not teach writing a first working data structure, copying the first working data structure in the memory space as a second working data structure, and writing the second working

data structure to the same memory space as the first working data structure, as recited in the claim. Although the Office Action contends that O'Neill purportedly teaches the indicated limitation, this contention is respectfully traversed.

O'Neill relates to implementing software updates on a computing device. O'Neill, abstract. More specifically, O'Neill describes a flash memory 1002, a random access memory (RAM) 1004, a section 1224 of the flash memory 1002, a section 1222 of the RAM 1004, a working bank 1232 of the RAM 1004, a backup bank 1234 of the flash memory 1002, and an original bank 1242 of the flash memory 1002. O'Neill, Fig. 12; page 18, paragraph 140, through page 19, paragraph 150.

Memory sections 1222 and 1224 are allocated in different memory devices

As stated in paragraph 140 of O'Neill, the section 1222 of the RAM 1004 is a first allocation of the RAM 1004 that is configured to temporarily store an update package 110. As stated in paragraph 142 of O'Neill, the section 1224 of flash memory is a first allocation of the flash memory 1002 configured to store a copy of the update package 110 from the section 1222 of the RAM 1004. In other words, as described in O'Neill, each of the sections 1222 and 1224 are different from one another. Additionally, the sections 1222 and 1224 are allocated in different memory devices, in the RAM 1004 and the flash memory1002, respectively. Therefore, no data that could be stored in the sections 1222 or 1224 could be stored in the same memory space as each other because the data stored in each section is stored on a different memory device. Although, O'Neill states that the data stored in the section 1222 is a copy of the data stored in the section 1224, as previously stated, the section 1222 is allocated in the RAM 1004 and the section 1224 is allocated in the flash memory 1002. Therefore, not only is the data stored in different allocations with regard to sections 1222 and 1224, but the data is stored in physically different memory devices. Hence, in regard to the sections 1222 and 1224, O'Neill does not teach writing a first working data structure and a second working data structure to the same memory space.

Banks 1232 and 1234 are allocated in different memory devices

In paragraph 145, O'Neill explains that in state 1230 "a plurality of memory allocation operations are performed." Additionally, as stated in paragraph 145 of O'Neill, the working bank 1232 of RAM 1004 is a second allocation of the RAM 1004 configured to act as an operational buffer or working memory area where operations determined by the instruction set are performed, and "a backup bank 1234 may be allocated... in the flash memory" (emphasis added). Thus, the backup bank 1234 of the flash memory 1002 is a second allocation of the flash memory 1002. Furthermore, in paragraph 145, O'Neill states, and that the bank 1234 may be configured to "serve as a backup copy of the data in instances where the data in the working bank 1232 may become corrupted or fail validation checks." As described by O'Neill, the bank 1234 of the flash memory 1002 may be configured to store a copy of the contents of the bank 1232 of the RAM 1004. In other words, as described in O'Neill, each of the banks 1232 and 1234 are separate allocations from one another. Additionally, the banks 1232 and 1234 are allocated in different memory devices, in the RAM 1004 and the flash memory1002, respectively. Therefore, none of the data that may be stored in the banks 1232 or 1234 could be stored in the same memory space as each other because the data stored in each bank is stored on a different memory device. Moreover, O'Neill states that the data stored in the bank 1234 is a copy of the data stored in the bank 1232. However, as previously stated, the bank 1232 is allocated in the RAM 1004 and the bank 1234 is allocated in the flash memory 1002. Therefore, not only is the data stored in different allocations with regard to banks 1232 and 1234, but the data is stored in different memory devices. Hence, in regard to the banks 1232 and 1234, O'Neill does not teach writing a first working data structure and a second working data structure to the same memory space.

Banks 1234 and 1242

As explained in paragraphs 148-150 of O'Neill, the contents of the bank 1232 in the RAM 1004 may be copied and written to the bank 1234 in the flash memory 1002. Additionally, the contents of the bank 1232 may be copied and written to the bank 1242 in the flash memory 1002. Hence, two separate banks in the same flash memory 1002

may contain copies of the same data in the RAM 1004. However, even though the two banks 1234 and 1242 in the flash memory 1002 may contain the same data, O'Neill does not teach copying the data in the bank 1234 of the flash memory 1002 and writing the contents of the bank 1234 to the bank 1242, where both banks are in the same memory device. Instead, O'Neill expressly states that the contents of the bank 1232 in the RAM 1004 are copied from the RAM 1004 and written to the bank 1234 in the flash memory 1002, and that the contents of the bank 1232 in the RAM 1004 are also copied from the RAM 1004 and written to the bank 1242 in the flash memory 1002. In other words, although the contents of the banks 1234 and 1242 may contain copies of the same data in the same flash memory device, O'Neill does not teach copying data from a bank in the same memory device and writing the copied data to the same memory space of the same memory device. Hence, in regard to banks 1234 and 1242 in the flash memory 1002, O'Neill does not teach a memory allocation unit adapted to allocate at least one first part of said memory space to write a first working data structure comprising a plurality of working data blocks to the memory space and to write a second working data structure comprising a copy of the plurality of working data blocks, as recited in the claim.

Additionally, the Office Action does not assert that Stockdale or Cheng might teach the missing limitation of O'Neill. Therefore, the combination of Stockdale, Cheng, and O'Neill fails to teach all of the limitations of the claim because O'Neill does not teach "a memory allocation unit adapted to communicate with at least one application device and to allocate at least one first part of said memory space to said application device to write a first working data structure comprising a plurality of working data blocks to the memory space and to write a second working data structure comprising a copy of the plurality of working data blocks, wherein the second working data structure comprises a copy of the first working data structure in the same memory space as the first working data structure," as recited in claim 1. Accordingly, Applicants respectfully submit that claim 1 is patentable over the combination of Stockdale, Cheng, and O'Neill because the cited references do not teach all of the limitations of the claim.

Independent Claim 5

Applicants respectfully assert independent claim 5 is patentable over Stockdale, Cheng, O'Neill, and Hanes at least for similar reasons to those stated above in regard to the rejection of independent claim 1. In particular, claim 5 recites "wherein the copy of the first working data structure is written to a same memory space as the first working data structure" (emphasis added).

Here, although the language of claim 5 differs from the language of claim 1 and the scope of claim 5 should be interpreted independently of claim 1, Applicants respectfully assert that the remarks provided above in regard to the rejection of claim 1 also apply to the rejection of claim 5. Additionally, the Office Action does not assert that Stockdale, Cheng, or Hanes might teach the missing limitation of O'Neill. Accordingly, Applicants respectfully assert claim 5 is patentable over Stockdale, Cheng, O'Neill, and Hanes because O'Neill does not teach a copy of the first working data structure is written to a same memory space as the first working data structure.

Independent Claim 7

Applicants respectfully assert independent claim 7 is patentable over Stockdale, Cheng, and O'Neill at least for similar reasons to those stated above in regard to the rejection of independent claim 1. In particular, claim 7 recites "wherein the copy of the first working data structure is written to a same memory space as the first working data structure" (emphasis added).

Here, although the language of claim 7 differs from the language of claim 1 and the scope of claim 7 should be interpreted independently of claim 1, Applicants respectfully assert that the remarks provided above in regard to the rejection of claim 1 also apply to the rejection of claim 7. Additionally, the Office Action does not assert that Stockdale or Cheng might teach the missing limitation of O'Neill. Accordingly, Applicants respectfully assert claim 7 is patentable over Stockdale, Cheng, and O'Neill because O'Neill does not teach a copy of the first working data structure is written to a same memory space as the first working data structure.

Independent Claim 10

Applicants respectfully assert independent claim 10 is patentable over O'Neill at least for similar reasons to those stated above in regard to the rejection of independent claim 1. In particular, claim 10 recites "a memory allocation unit… to allocate at least one first part of said memory space to said application device to write a first working data structure comprising a plurality of working data blocks to the memory space and to write a second working data structure comprising a copy of the plurality of working data blocks… wherein the second working data structure comprises a copy of the first working data structure in the same memory space as the first working data structure" (emphasis added).

Here, although the language of claim 10 differs from the language of claim 1 and the scope of claim 10 should be interpreted independently of claim 1, Applicants respectfully assert that the remarks provided above in regard to the rejection of claim 1 also apply to the rejection of claim 10. Additionally, the Office Action does not assert that Stockdale or Cheng might teach the missing limitation of O'Neill. Accordingly, Applicants respectfully assert claim 10 is patentable over O'Neill because O'Neill does not teach the recited limitations.

Independent Claim 11

Applicants respectfully assert independent claim 11 is patentable over Stockdale, Cheng, O'Neill, and Hanes at least for similar reasons to those stated above in regard to the rejection of independent claim 1. In particular, claim 11 recites "allocating at least one first part of said memory space to a file system device, writing a first working data structure comprising a plurality of working data blocks to the memory space, writing a second working data structure comprising a copy of the plurality of working data blocks, wherein the second working data structure comprises a copy of the first working data structure in the same memory space as the first working data structure" (emphasis added).

Here, although the language of claim 11 differs from the language of claim 1 and the scope of claim 11 should be interpreted independently of claim 1, Applicants respectfully assert that the remarks provided above in regard to the rejection of claim 1 also apply to the rejection of claim 11. Additionally, the Office Action does not assert that Stockdale, Cheng, or Hanes might teach the missing limitation of O'Neill.

Accordingly, Applicants respectfully assert claim 11 is patentable over Stockdale, Cheng, O'Neill, and Hanes because O'Neill does not teach the recited limitations.

Dependent Claims

Claims 2-4, 6, 8, and 12-25 depend from and incorporate all of the limitations of the corresponding independent claims 1, 5, 7, and 11. Applicants respectfully assert claims 2-4, 6, 8, and 12-25 are allowable based on allowable base claims. Additionally, each of claims 2-4, 6, 8, and 12-25 may be allowable for further reasons.

CONCLUSION

Applicants respectfully request reconsideration of the claims in view of the remarks made herein. A notice of allowance is earnestly solicited.

At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account **50-3444** pursuant to 37 C.F.R. 1.25. Additionally, please charge any fees to Deposit Account **50-3444** under 37 C.F.R. 1.16, 1.17, 1.19, 1.20 and 1.21.

Respectfully submitted,

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